Design Engineering

ISSN: 0011-9342

Issue: 11 | Pages: 815 - 823

Research on Improved D-NPC Three Phase Three Level Converter and Its Control Strategy

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Abstract:

Diode Neutral Point Clamped (D-NPC) three-level topology with simple structure and low withstand voltage of single power device is suitable for medium voltage applications. Due to the long working time and high temperature of the inner tube in the main bridge arm of the d-npc structure, the design of the radiator is difficult, and the output current and switching frequency are limited. In order to solve this problem, this paper proposes an improved d-npc three-phase three-level topology, optimizes the traditional seven segment SVPWM modulation strategy, builds a simulation model based on PMSM control device, and proves the correctness and feasibility of the improved structure.

Keywords*: D-NPC, SVPWM, FPGA, three-level converter, control strategy.*

I. INTRODUCTION

In the promotion of new energy automobiles, especially pure electric vehicles, the core control device of energy flow conversion has become the research focus [1]. Compared with the two-level converter, the multi-level converter adopts more electric levels, and the waveform quality is optimized by reducing the output voltage drop ratio and switching loss. At present, the main structure of multi-level converter is cascaded type and mid-point clamp type. The earliest form of neutral point clamped is a FC-NPC (Flying Capacitor Neutral Point Clamped). According to the structural characteristics of FC-NPC, the capacitor is replaced by a two-way switching power device as a midpoint clamping element, and it is similar to letter “T”, so it is

ISSN: 0011-9342

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called T type Neutral Point Clamped (T-NPC). Based on the topologies of T-NPC and FC-NPC, the diode clamp multilevel topology is proposed. The main control circuit is simple, the control mode is flexible, and the energy flow direction and power factor are easy to control, which are the main advantages of the multilevel converter with diode clamp.However, due to the inherent control and driving mode of D-NPC, its heat loss is not uniform, which makes the design of the radiator more difficult, and the power level, output current and switching frequency limited. The Active Neutral Point Clamped (A-NPC) multilevel topology proposed later can improve the loss distribution, but its conduction loss and switching loss are relatively large [2]. After studying the characteristics of traditional D-NPC topology, an Improved Diodes Neutral Piont Clamped (D-NPC) structure was proposed, with more uniform distribution and simpler way to control and drive.

The D-NPC was proposed in 1980, and it is suitable for the occasions with a medium voltage. Its topological structure is shown in Figure 1 below [3-4], and each group of main bridge arms consist of four controllable switch elements and two diode clamped elements. The DC power supply is composed of two groups of AC sources in series with a monomer voltage of $\frac{V_{\mathrm{dc}}}{2}$, and the midpoint of DC source is connected with the midpoint of the series diode. Taking the first group of main bridge arms as an example, when the first switch element Q1-1 and the second switch element Q1-2 of the four switch elements of the main bridge arm are switched on, the phase output is $\frac{V_{\mathrm{dc}}}{2}$(known as positive level state).When the second switching element Q1-2 and the third switching element Q1-3 are switched on, the phase output is 0 (known as zero level state); When the third switching element Q1-3 and the fourth switching element Q1-4 are switched on, the phase output is $-\frac{V_{\mathrm{dc}}}{2}$(known as negative level state). Four controllable switching elements take turns to be on to make the output present a three-level state. In the switching process from positive level to zero level and from zero level to negative level, the second and third switching elements are in repeated conducting state, that is, continuous working state, and the heat distribution on a single device is not uniform [5]. As each set of main bridge arms has four switch control elements, and each switch control element needs one drive circuit, so a single set of converter needs 12 switch drive circuits [6].

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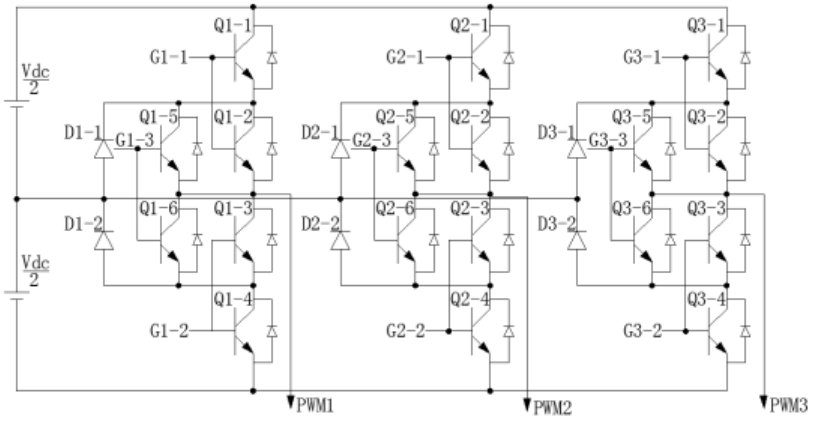

Figure 1 Topology of D-NPC

II. ID-NPC

The topology structure of the ID-NPC is shown in Figure 2 below. Each group of main bridge arms consist of six controllable switch elements and two diode clamped elements .The DC power supply and converter are connected in the same way as the D-NPC. Taking the first group of main bridge arms as an example, when the six switch elements of the main bridge arm are divided into three groups: Q1-1 and Q1-2, Q1-3 and Q1-4, Q1-5 and Q1-6, the driving portsare G1-1, G1-2 and G1-3, respectively. When the driver port G1-1 is switched on, the phase output is$\frac{V_{\mathrm{dc}}}{2}$ (positive level state); When the driver port G1-2 is switched on, the phase output is 0 (zero level state); When the driver port G1-3 is switched on, the phase output is $-\frac{V_{\mathrm{dc}}}{2}$(negative level state).Three sets of six controllable switch elements take turns to be switched on to make the output present a three-level state. At this point, the positive level state, zero level state and negative level state are independent conduction elements, without repeated conduction superposition conduction state, and the heat distribution on a single device is uniform. The six three switch control elements of the main bridge arm need three drive circuits, and a single converter needs nine switch drive circuits.

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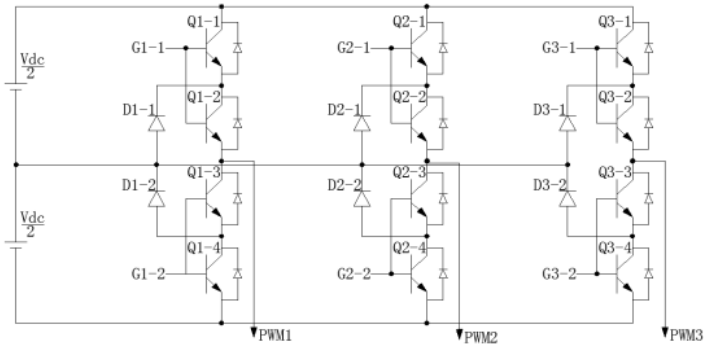

Figure 2 Topology of ID-NPC

III. Optimization of control strategy

In this paper, the control strategy is implemented in MATLAB Simulink environment based on the Xilinx System Generator, and the optimization principle is to save hardware resources to the maximum extent under the premise of balanced speed and function.The simulation module is divided into four parts: 3-2 transformation module, size area judgment module, action time calculation and selection module, state selection module and switch output module.

3.1 3-2 Transformation Module

The input three-phase wave voltage is driven by rotating clockwise, as shown in the following formula:

$$\begin{cases} u_a = V_m \cos(\theta) \\ u_b = V_m \cos\left(\theta - \frac{2}{3}\pi\right) \\ u_c = V_m \cos\left(\theta + \frac{2}{3}\pi\right) \end{cases} \quad (1)$$

The transformation from natural coordinate system to static coordinate is as follows:

$$\begin{cases} u_\alpha = M \times \frac{3}{2} V_m \cos(\theta) \\ u_\beta = M \times \frac{3}{2} V_m \sin(\theta) \end{cases} \quad (2)$$

The coefficient$M = \frac{2}{3}$is conducted with the same altitude transformation. In consideration of saving FPGA hardware resources, sines and cosines are obtained by using 12-bit depth lookup

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ISSN: 0011-9342

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table (LUT) [7].

3.2 Size Area Judgment

Based on the 12-bit depth lookup table, it is divided into six large regions corresponding to $0\sim4096$ equal differences according to linear $0\sim2\pi$, and each large region is further divided into six small regions.m $=\frac{\sqrt{3}U_{ref}}{V_{dc}}$, where U_{ref} is the vector module in static coordinates, as shown in Figure 3.The conversion method takes the first region DOF as an example, and the other five regions are similar. The vectors $\overrightarrow{U_{ref1}}$and $\overrightarrow{U_{ref}}$ are located in the DOF region, with an argument of θ, and module is $U_{ref1}$and U_{ref}, where $U_{ref1}=2U_{ref}$. When the vector $\overrightarrow{U_{ref1}}$is located in the trapezoidal regionACFD, $\overrightarrow{U_{ref1}}=2U_{ref}e^{j\theta}$, and after transformation, the vectors in the trapezoidal regionACFD can be expressed as two times of the vector mode of the same argument in the triangle region. This method greatly simplifies the regional selection process, improves the regional selection, and saves the regional judgment time and system resources.

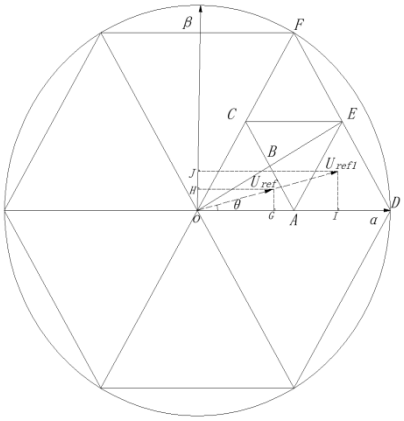

Figure 3 Three-level space voltage vector diagram

3.3 Action Time Calculation and Selection

The equivalent reference voltage vector is synthesized by using adjacent fundamental vectors, and the action time of the basic vector is determined according to the principle of volt-second equilibrium. According to Figure 3, DOF area is marked as Ⅰ, other areas are marked by counterclockwise as Ⅱ, Ⅲ, Ⅳ, Ⅴ, Ⅵ. Region Ⅰ of the first major area is

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composed of six small regions, including AOB, BOC, DAE, EAB, EBC, and ECF , which are marked as I_1, I_2, I_3, I_4, I_5, and I_6, and the marking methods of small and medium-sized areas in other large areas are similar. The vectors in each small region are synthesized by the action of three adjacent basic vectors, which correspond to three action time values T_1, T_2, and T_3, respectively, so the corresponding time values of the basic action vectors in 36 small regions are 108, among which, T_1, T_2, and T_3in Ⅰ, Ⅲ, and Ⅴ are the same, T_1, T_2, and T_3in Ⅱ, Ⅳ, Ⅵ are the same, and the time values can be simplified into 36.Those with same or opposite time values are categorized into one value, and the 36 time values are simplified into 7. After further simplification, they are finally simplified into 3 cosine values:$\cos(\theta)$,$\cos(\frac{\pi}{3}-\theta)$, and$\cos(\frac{\pi}{3}+\theta)$.Through the above optimization, the table lookup method is used to represent the required 108 time values by using only three cosine function values, which equalizes the balance between time and resources.

3.4 State Selection and Switch Output

To be better equivalent to the synthetic reference vector, a more effective seven-stage time state allocation method is adopted. The shorter vector is used as the starting vector when the three adjacent basic vectors act on. The state selection follows that only one phase circuit state changes when the voltage vector changes, which minimizes the switching loss.

IV. SIMULATION ANALYSIS

Simulation conditions: DC side voltage$V_{dc} = 1000\text{V}$, sampling frequency$f_{Ts} = 10\text{KHz}$, simulation time$T = 0.4\text{s}$, input frequency$f_{out} = \frac{f_{TS}\times\delta}{2^{12}} = \frac{1\times10^4\times20}{2^{12}} = 48.8\text{Hz}$ (δ is the input frequency control quantity), load torque$T_L = 20\text{N}\cdot\text{m}$, $m = 0.8$, and other parameters are defaults [8].

PMSM motor parameters: stator resistance $R = 0.958\Omega$, armature inductance $L_d = 0.00525\text{H}$, $L_q = 0.0012\text{H}$, flux linkage$\psi_f = 0.1872\text{Wb}$, rotational inertia$J = 0.003\text{Kg}\cdot\text{m}^2$, and damping coefficient$B = 0.008\text{N}\cdot\text{M}\cdot\text{s}$.

A. The revolving speed waveform is shown in Figure 4. Figure 4 (a) shows the revolving speed waveform of D-NPC and Figure 4 (b) shows the revolving speed waveform of ID-NPC. It can be seen from the figures that the revolving speed of the two waveforms approach 77rad⁄s.

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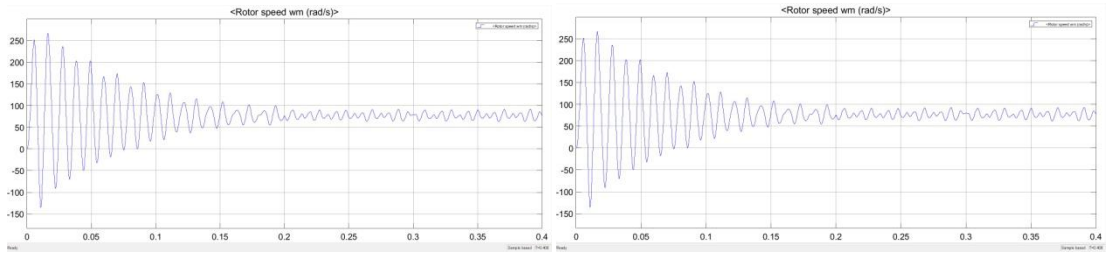
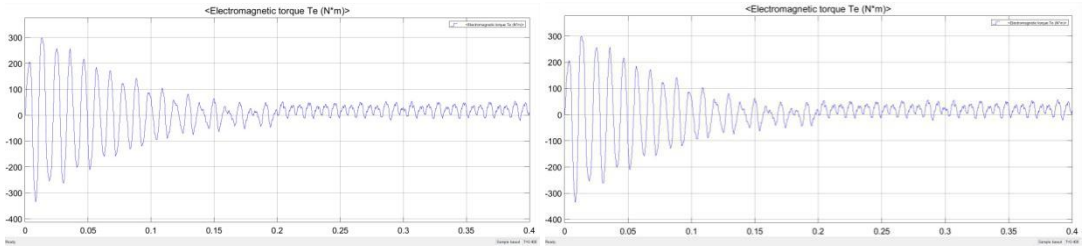


(a) (b)

Figure 4 Rotational speed waveform

B. The electromagnetic torque waveform is shown in Figure 5. Figure 5 (a) shows the electromagnetic torque waveform of D-NPC and Figure 5 (b) shows the electromagnetic torque waveform of ID-NPC.



(a) (b)

Figure 5 Waveform of electromagnetic torque

C. The rotor's phase current waveform is shown in Figure 6. Figure 6 (a) shows the DNPC phase current waveform and Figure 6 (b) shows the ID-NPC phase current waveform. It can be seen from the waveform of the both is basically consistent.

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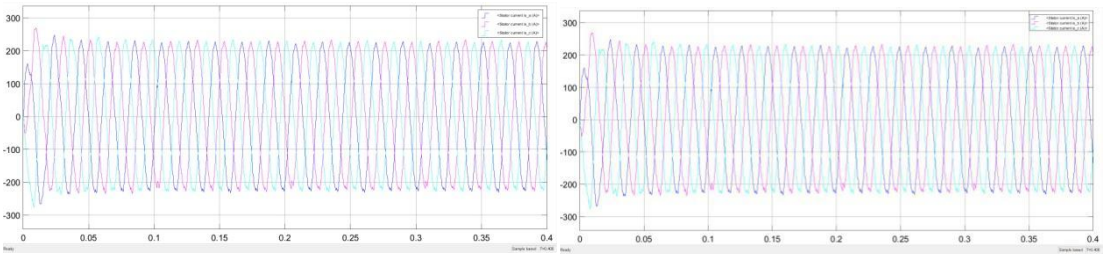
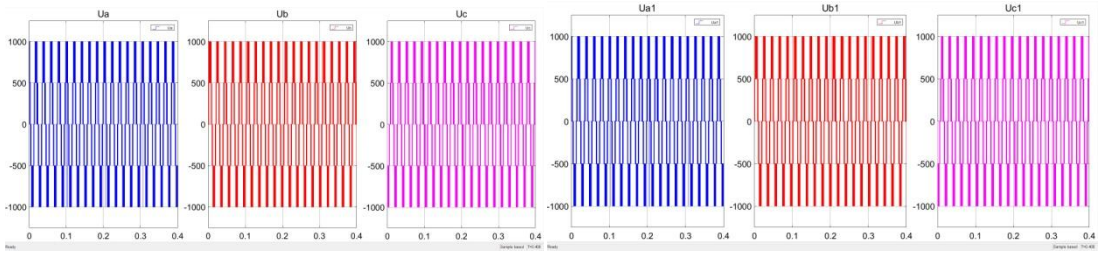


(a) (b)

Figure 6 Waveform of phase current

D. The waveform of phase voltage is shown in Figure 7. Figure 7 (a) shows the waveform of ABC phase voltage of D-NPC structure, and Figure 7 (b) shows the waveform of ABC phase voltage of ID-NPC structure, and the waveform of the both is similar.



(a) (b)

Figure 7 Waveform of phase voltage

V. CONCLUSION

Power electronic converter is an important device for the flow conversion of variable frequency speed regulating motor. In this paper, through studying traditional D-NPC structure converter, an improved ID-NPC converter is proposed, and in view of the problems of the traditional SVPWM control strategy, such as complex implementation and large consumption of hardware and software resources, the converter's switch control strategy is further optimized, the simulation environment based on quickness and the real-time FPGA structure is made full use of to prove the correctness and feasibility of the proposed method.

ISSN: 0011-9342

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